WHAT IS CLAIMED IS:

1. A semiconductor memory device connected between a processor and an instruction cache, comprising:

an instruction buffer storing part of consecutive instructions performed by the processor;

an address table setting therein an address range of the part of the consecutive instructions;

a determination unit determining whether an instruction address outputted from said processor fall within the address range set in said address table; and

a selector selectively outputting an instruction code stored in said instruction buffer and an instruction code stored in said instruction cache in accordance with a determination result of said determination unit.

2. The semiconductor memory device according to claim 1, wherein

said determination unit directly connects said processor and said instruction cache when an inactive mode is set.

3. The semiconductor memory device according to claim 1, wherein

said address table and said instruction buffer are mapped on a memory map of said processor, and operate as a memory mapped device when an inactive mode is set.

4. The semiconductor memory device according to claim 1, wherein

said determination unit includes:

a first subtracter subtracting a maximum value of address set in said address table from the instruction address outputted from said processor;

a second subtracter subtracting a minimum value of the address set in said address table from the instruction address outputted from said processor; and

a logic circuit determining whether the instruction address outputted from said processor fall within the address range set in said address table

in accordance with a sign of a subtraction result of said first subtracter and a sign of a subtraction result of said second subtracter.

5. The semiconductor memory device according to claim 4, wherein said second subtracter outputs the subtraction result to said instruction buffer as an address.

6. The semiconductor memory device according to claim 4, wherein said determination unit further includes a comparator comparing upper bits of the instruction address outputted from said processor with upper bits of the maximum value set in said address table, and stopping operations of said first subtracter and said second subtracter in the case of determining inconsistency of the upper bits.

7. The semiconductor memory device according to claim 4, wherein in the case of determining that the instruction address outputted from said processor fall within the address range set in said address table, said logic circuit stops an operation of said second subtracter until it is determined that the instruction address outputted from said processor is out of the address range set in said address table.

8. The semiconductor memory device according to claim 7, wherein the instruction address outputted from said processor is supplied as addresses of said instruction buffer.

9. A software development apparatus for a processor system including a semiconductor memory device connected between a processor and an instruction cache and storing part of consecutive instructions performed by said processor, the software development apparatus comprising:

an extraction section extracting consecutive instructions arranged in said semiconductor memory device from a source file;

an acquisition section acquiring address information on addresses at

which the consecutive instructions extracted by said extraction section is originally mapped;

a reformatting section reformatting the address information acquired by said acquisition section into a form compatible with said source file; and

a generation section generating a load module from said source file, the consecutive instructions extracted by said extraction section, and the address information reformatted by said reformatting section.

10. The software development apparatus according to claim 9, wherein

said extraction section extracts consecutive instructions designated by a predetermined a reserved symbol from said source file, and sets the extracted consecutive instructions as the consecutive instructions arranged in said semiconductor memory device.

11. The software development apparatus according to claim 9, wherein

said extraction section extracts common consecutive instructions from said source file, and sets the extracted common consecutive instructions as the consecutive instructions arranged in said semiconductor memory device.

12. The software development apparatus according to claim 9, wherein

said acquisition section extracts lower bits of a top address of the consecutive instructions from the acquired address information, and shifts the addresses of the consecutive instructions by as much as the number of bytes corresponding to the lower bits of the top address.

13. The software development apparatus according to claim 9, wherein

said generation section sets a branch instruction to branch to a top of a reserved region preset in a main memory, to a top address of a region of

said main memory corresponding to the consecutive instructions extracted by said extraction section, and

said generation section adds a branch instruction to branch to an instruction right after an end address of the region of the main memory corresponding to the consecutive instructions, to an end of the consecutive instructions extracted by said extraction section.